APV-25 based readout electronics for the SBS front GEM Tracker

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Version: 1.0

1.1 Changelog

Version 0.1: first version

Version 0.2: added section on connection topology; included estimation of front end electronics based on EES formal offer.

Version 1.0: integrated comments and suggestion by N. Liyanange

1.2 Introduction

This document is a short summary on the readout electronics developed for the readout SBS GEM front trackers, which is commonly referred as MPD-INFN electronics, and it has to be considered as an attachment to the report “APV-25 readout system options for the SBS back GEM tracker” by K. Gnanvo and N. Liyanange.

The MPD-INFN readout electronics is based on the APV25 chip developed by the Imperial College for CMS silicon detectors and firstly used in a GEM detector by COMPASS. In the last few years has been adopted by HADES for the readout of the MWPC of its RICH detector (in place of the slower Gassiplex).

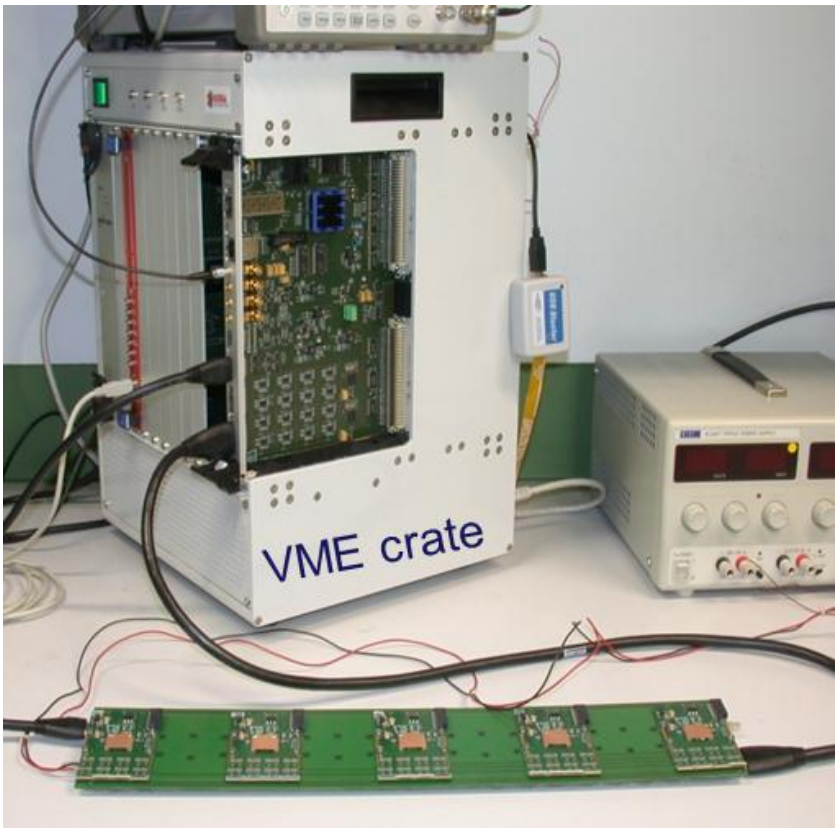

Figure 1: MPD-INFN system components: the front end card (FEC), the backplane that can host up to 5 cards, the VME controller in VME64x standard; cards and MPDs communicate by HDMI cables.

The electronics system consists of three main components (see Figure 1):

1. The front-end cards hosting the APV25 chip;
2. The backplanes that represent a passive electronic part and at the same time the mechanical support of the front-end cards; it hosts two radiation tolerant (to what level ?) voltage regulators ST-LHC4913 that supply the proper voltage levels to the front end cards;
3. The VME64x/VXS module (MPD – Multi Purpose Digitizer) that controls the front-end cards and acquires the analog signals coming from them. The VME module is in 64x standard according to the JLab DAQ standard.

The APV25 is designed to be radiation tolerant (at least 10 Mrad) . The voltage regulator LHC4913 passed without noticeable degradation the irradiation by 137Cs source for a total of 0.36 Mrad corresponding approximately to 4.5 JLab-year of operation (the regulator radiation hardness is expected to be much larger). All other passive components of the front-end cards and backplanes are expected to be radiation tolerant at the level of the APV25 at least.

The backplane and the MPD are connected by 2 HDMI-A cables, one for the digital signals, and the other for the analog output coming from the cards.

Figure 2 shows the layout of the electronics on a GEM front chamber; the green PCBs represent the backplanes; front end cards are below them. In the original design the MPD modules are placed at few tens of meters from the detectors, in a radiation shielded area. The noise issue of the APV25 and length of the HDMI cables may require placing the MPDs closer to the detector (compatible with <=6 m long HDMI cable).

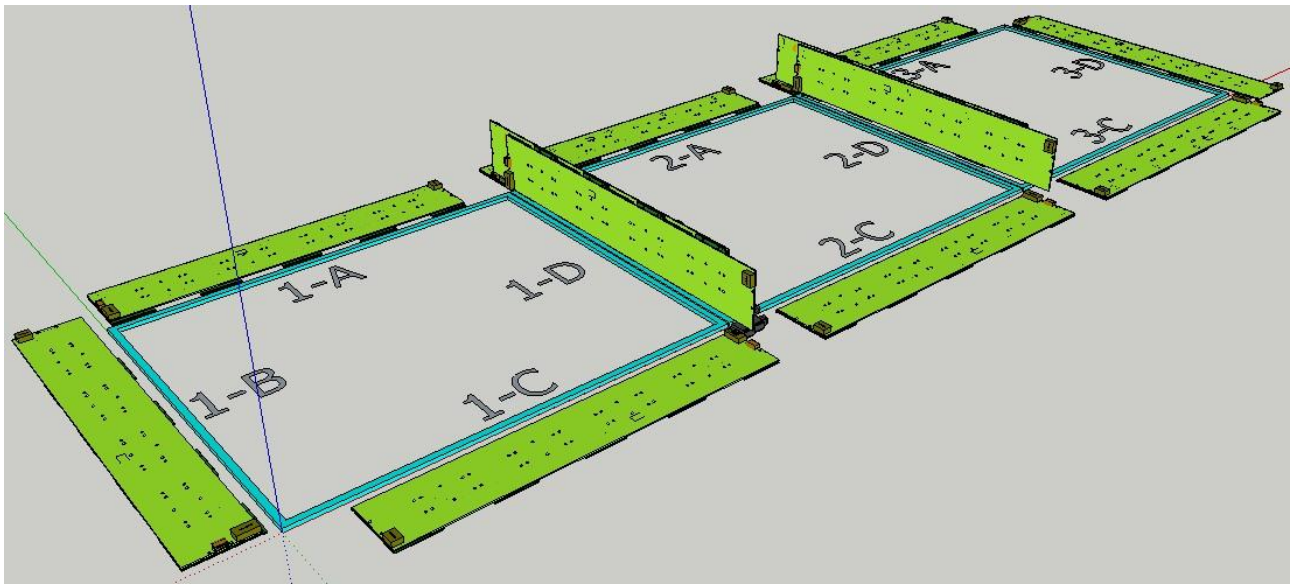

Figure 2: Electronics layout in a chamber, on plane all around the 3 modules and vertical between modules; the green PCB are the backplanes.

A version with Panasonic connectors on the front end cards and a different backplane has been designed and produced (prototype samples) for the SBS back GEM tracker.

The MPD-INFN electronics and the SRS electronics share many common design solutions; the main difference is the adoption of different standards for the controller/digitizer module and consequently different connection topologies and DAQ readout.

1.2.1 The Multi-Purpose Digitizer (MPD) module

The VME64x/VXS MPD module hosts an Altera ARRIA GX FPGA and can control/readout up to 16 APV cards for a total of 2048 channels. The FPGA handles:

- VME interface (VME64x with VXS extension and JLab custom multiblock transfer).
- ADS5281 interfacing (2 x 8 channels, up to 50 MHz (40 MHz typical), 12 bit ADC, with DDR serial interface @ 480 Mbit/s).
- I^2C protocol for on-board devices and APV25 configuration.
- APV25 triggering.
- Coaxial front panel I/O with configurable levels (LVTTL – NIM).
- Large memory buffer implemented with external DDR SDram (2 x Micron MT46V64M8: 128 M x 8 bits)

- Micro SD-Card interface (version 4.0)
- Ethernet 10-100 MAC (to be implemented in firmware).
- High speed optical protocol using SFP transceiver (to be implemented in firmware).
- User configuration switches, LEDs, ...
- Expansion PMC connectors.

The module only uses the +5V and therefore can be used in a standalone way (without the VME crate) once either the copper wired Ethernet or the optical fiber communication is implemented.

The VME64x standard has been adopted to be compliant to the JLab DAQ main framework.

The current implementation of the FPGA firmware also includes: Common noise suppression (by mean or median), pedestal subtraction, sparse readout.

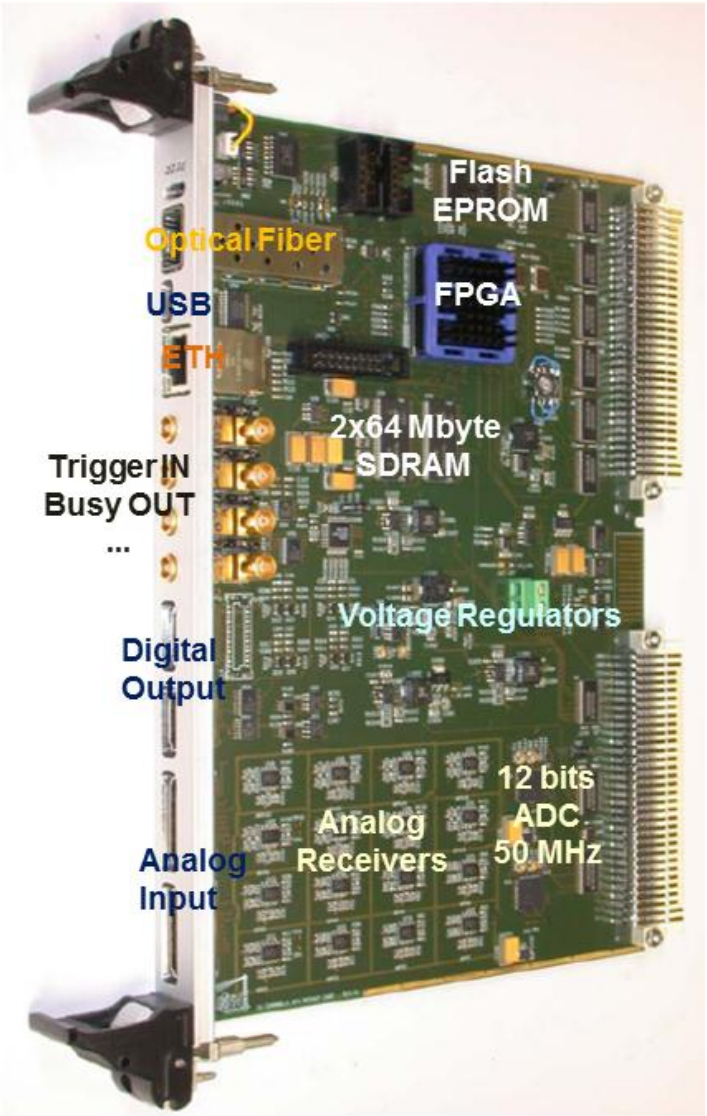

Figure 3: VME custom module MPD (Multi-Purpose Digitizer, version 3) for the control and readout of the front-end cards.

1.3 Performance

Noise

The typical pedestal RMS's (after common noise subtraction) under recent beam test with the final electronics on 40x50 cm2 front tracker GEM module are shown in Figure 4 and Figure 5. Noise level is sensitive to the different environmental conditions (typical noise in Rome laboratory is 2-3 ADC unit smaller) and to the length of the HDMI analogue cables (in particular the noisy channels at the beginning and the end of the APV-25 frame are the most sensitive to the HDMI cable length); with 3 meter long cables the noise drops down by about 2-3 ADC units.

One single ADC unit corresponds approximately to 150-200 electrons.

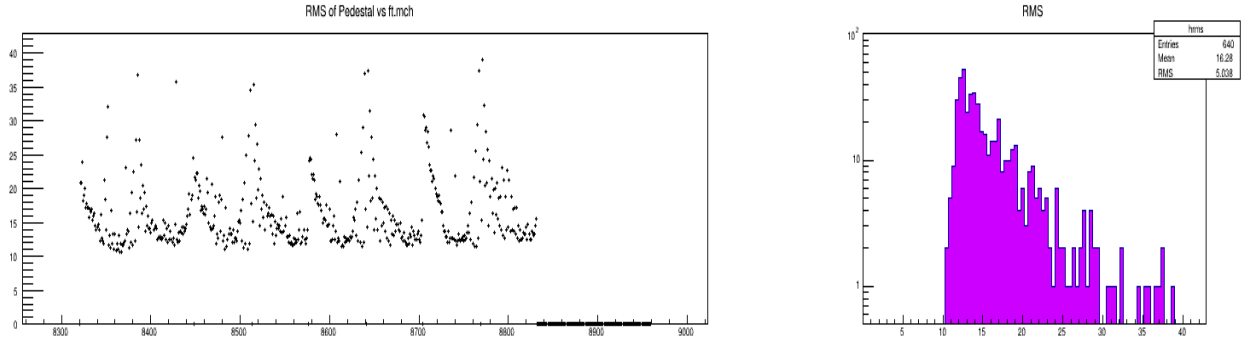

Figure 4: RMS pedestals for 4 cards connected to the x strips (50 cm long strips) in beam test environment (DESY/2014); average noise level is 16.2 ADC units; the analogue HDMI cable is 6 meter long.

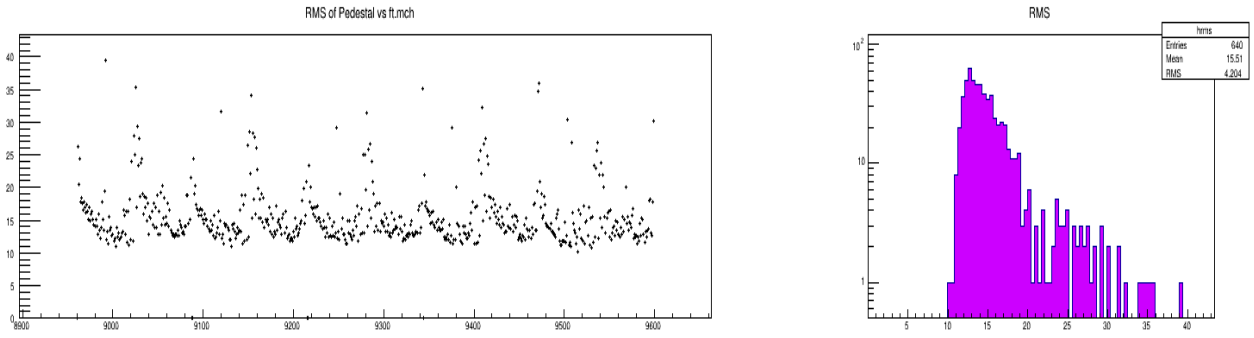

Figure 5: RMS pedestals for 5 cards connected to the y strips (40 cm long strips) in beam test environment (DESY/2014); average noise level is 15.5 ADC units; the analogue HDMI cable is 6 meter long.

Signal Amplitude

Figure 6 shows an example of hit distribution (single hit) with signal time evolution (6 samples) on a 40x50 cm2 GEM module for electrons of 2 GeV.

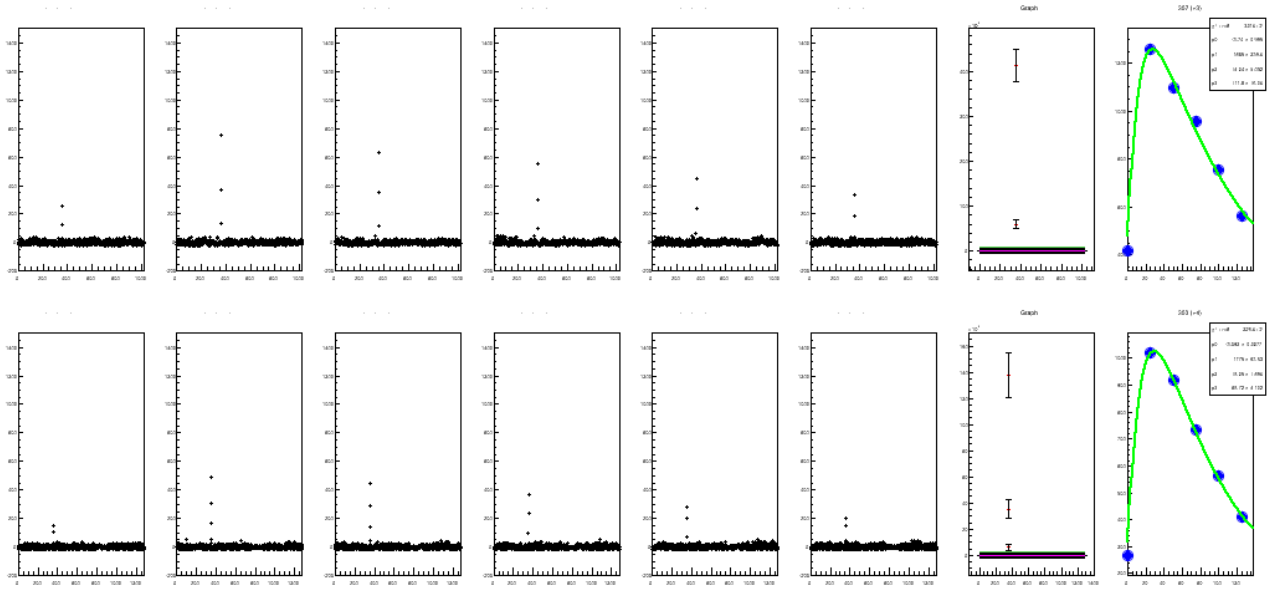

Figure 6: Event on a 40x50 cm2 GEM module from the DESY Test Electron Beam. The two rows report the x and y strips respectively on the abscissa. The first 6 columns represent the 6 collected samples, with 25 ns sampling period. The 7th column represents a combination of the first three columns to enhance the hit detection. The last column shows the charge of the hit in the six samples and the result of the fit presented later in the text for the estimation of the signal timing.

In Figure 7 are reported the typical distributions of the maximum ADC of a single strip (x and y), with GEM module HV at 4100 V, corresponding to a gain of approximately 5000 (from COMPASS parameterization) for MIP electrons (2 GeV energy). Saturation is barely visible above 1400 ADC units.

Signal Timing

Timing performances of the APV signal are reported in Figure 8, where 6 APV samples are fit by the function: $A[1-\exp[(t_0-t)/\tau_0]]\exp[(t_0-t)/\tau_1]$ for t>t_0 and 0 for t<=t_0. t_0 represents the start time of the signal (with opposite sign in the plots); τ_0 and τ_1 the raising and leading time constants. The small RMS of t0 need to be further investigated; the RMS of t0 seems to be independent (within error) from the point where the particle cross the chamber.

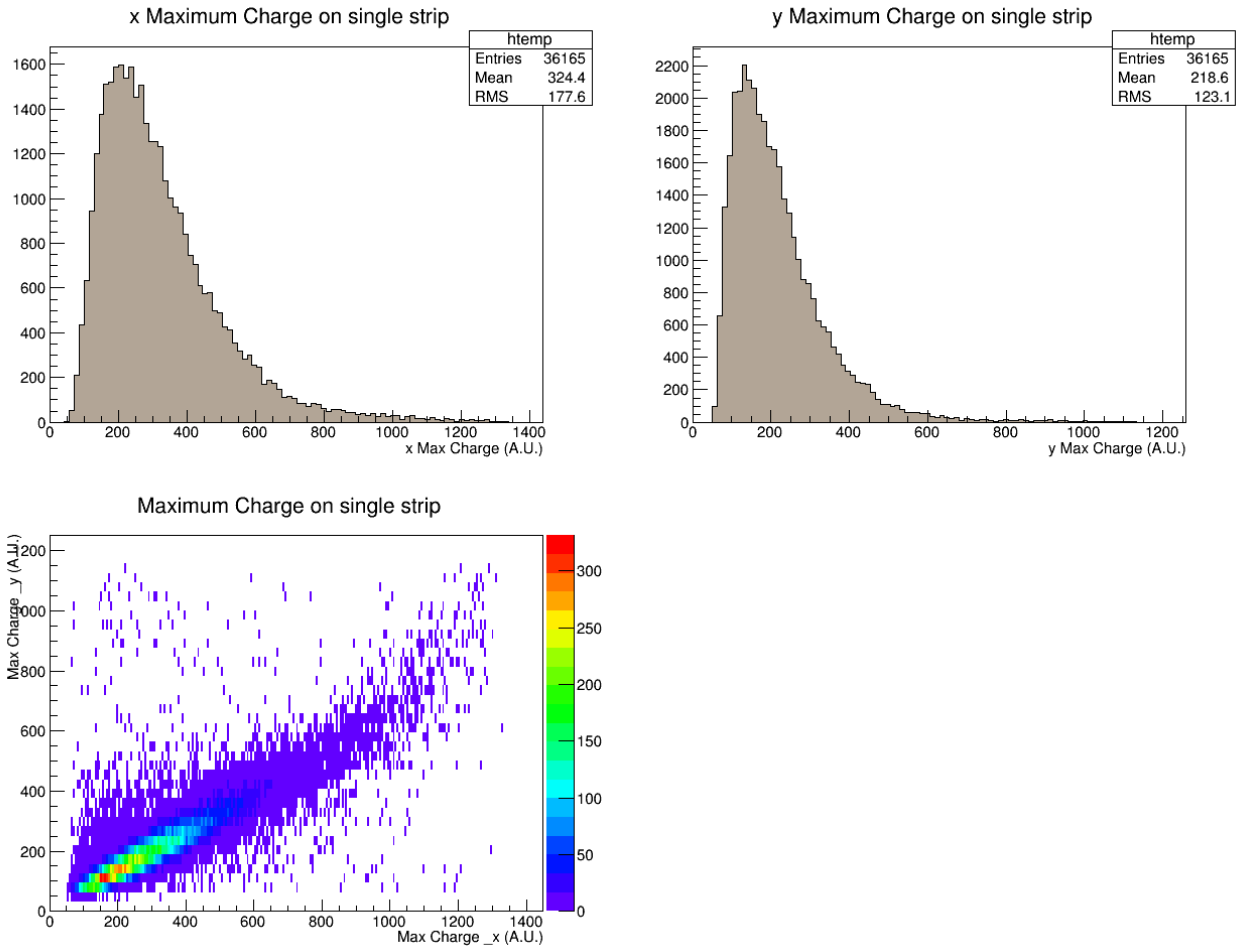

Figure 7: ADC distribution (x and y strips) for the strip with maximum charge, obtained with a HV of 4100 V (gain of approx. 4800).

Readout rate

The event size of a single APV (128 channes), one sample, is 0.4 kByte (without sparse readout).

The module maximum transfer rate over the VME64x bus is 100 Mbyte/s while on the Optical Fiber can approach 300 Mbyte/s.

The maximum transfer rate over the VME64x bus is 200 Mbyte/s; this usually represents the bottleneck of the acquisition speed.

There are enough FPGA resources to use the optical fiber either as a fast Ethernet connection or implementing the simple AURORA protocol used by the JLab/SSP modules. In either case the optical fiber can be used to parallelize the transfer of the data and therefore eliminate the bottleneck of the VME64x shared transfer.

1.4 Connection Topology

In the original design, the MPD-INFN electronics is expected to be connected as follow:

- The APV front end boards are directly connected to backplanes (up to 5 cards on one backplane), by means of PCB mounted mini connectors.
- The backplanes are connected to HDMI adapters (passive rerouting PCBs, both for digital and analogue signals) by 3 m long HDMI-A cables; one digital adapter connects up to 3 backplanes; one analogue adapter connects up to 3 backplanes.
- The adapters are connected to the MPDs by 20 m long HDMI-A cables; 2 cables for each digital adapter, 4 HDMI-A cables for each analogue adapter.
- The MPDs seats in VME64x/VXS crates far from the high radiation area.

If either the optical fiber or Ethernet interface is adopted, a different topology will be likely used: the MPDs can be moved closer to the APV front-end+backplanes, avoiding the 20 m long HDMI-A cables; the MPDs can be hosted in inexpensive, small crates, which will provide the 5 V power supply only (and mechanical support); the MPDs still need to be shielded from high radiation background. The MPDs can be connected, for example, to the JLab/SSP modules via optical fibers; a single SSP can likely manage from 8 up to 16 MPDs and do some further processing of the data. Detail of the SSP-MPD interface and topology as well as maximum rate capability need to be investigated together with the JLab engineers.

1.5 Development

The hardware design of the MPD-INFN readout electronics is consolidated; only minor reworking is possible (if needed). Most of the current development is oriented to the firmware of the FPGA with the completion of the VXS JLab protocol, the implementation of the fiber optics communication protocol, and possible improved sparsification that take into account the signal start time and its correlation with the trigger.

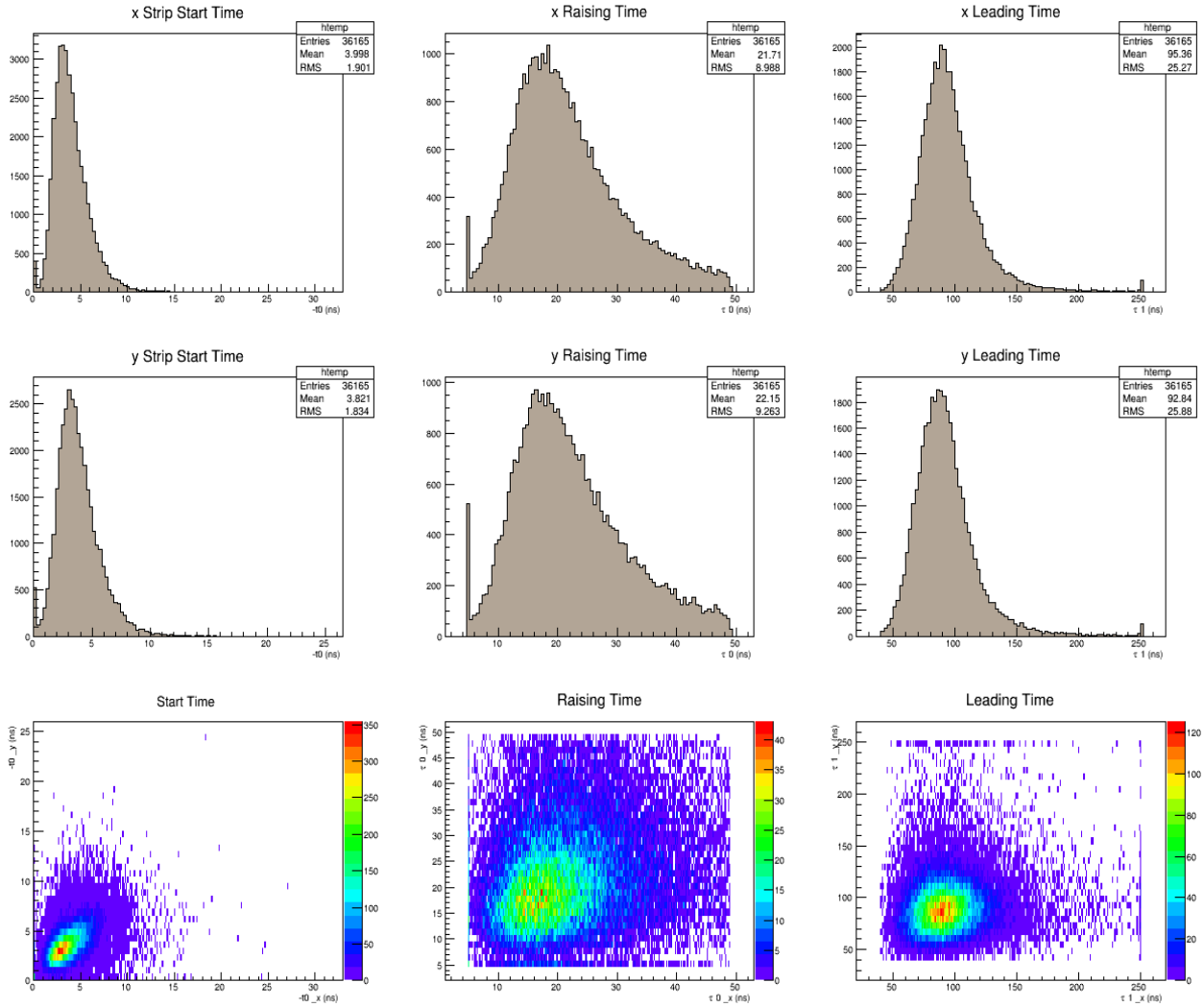

Figure 8: Timing characteristics from 6 APV samples fitting: left column represents the x and y strips start time (relative to the trigger) distribution; note values are negated for better plotting (0 and 25 ns are the fit boundaries); middle column the raising time constant (5 and 50 ns are fit boundaries) for x and y strip signals; right column leading time constant (40 and 250 are fit boundaries) for x and y strip signals; the bottom row shows the scatter plots of the above rows. Cuts on the quality of the fit (Chi2 and raising and lading times within boundaries) are applied (about 70% of events survived the cuts). Chamber operated at 4100 V.

1.6 Cost and system availability

The following table summarizes the total expected costs for a complete system.

Item	Amount	Item cost Euro	Item Cost	Total
APV card	530	€ 71.50	$97	$51,158
APV bonding	530	€ 28.00	$38	$20,034
Backplanes	106	€ 80.70	$109	$11,548
MPD units	36	€ 1,911.00	$2,580	$92,875
HDMI Adapter	72	€ 35.00	$47	$3,402
HDMI long cables	240	€ 50.00	$68	$16,200
HDMI short cables	240	€ 8.00	$11	$2,592
LV power channels	900	€ 10.00	$14	$12,150
VME crates	4	€ 10,490.00	$14,162	$56,646
VME controller	4	€ 4,196.00	$5,665	$22,658
Manpower: post-doc FTEY	0.5		$90,000	$45,000
Total				$334,263

The price of the APV chip (27 CHF) is from an old order for the front tracker.

The costs of APV bounding, APV Front End Board, Backplane and MPD come from the EES Company formal invoice and do not include VAT, custom duties and transportation.

The costs of HDMI adapter, HDMI Long Cable, HDMI Short Cable, LV Power Supply come from the front-tracker already ordered items (different prices may apply in US). The unit cost of LV Power Supply is expressed in euro/Watt, and the average power consumption of a single APV front-end+backplane is 1.5 W, for a total of 900 W.

The costs of VME crate and VME controller come from JLab estimation.

We assumed the original design with long HDMI-A cable; each MPD manages and acquires 15 cards. Each VME crate hosts up to 11 MPDs (which should permit the proper data transfer rate at about 50% occupancy, 5 kHz trigger rate).

If the optical fibers are adopted, a different connection topology will be used (as described above); in this case, we expect that the significant reduction of the costs of cabling and VME crates/controllers will compensate the extra costs of JLab/SSP modules (3 are expected to be needed), fibers and 5V power supplies for MPDs. We have no estimate on required extra shielding.

The front tracker electronics readout (41472 channels + spares) is partially completed; backplanes and MPD have been produced. Within June 2014 all readout cards will be delivered. Within the end of fall 2014 all electronics for the front tracker will be tested.

According to EES communication, the back tracker MPD based electronics can be provided by EES within 7 months (5 months without bounding) from order.